What is claimed is:

1. A method of producing a uniform wafer thickness profile in a polishing operation, comprising:

a) providing a model for a wafer polishing that defines a plurality of regions on a wafer and identifies a wafer material removal rate in a polishing step for each of the regions; and

(b) polishing a wafer using a polishing recipe that generates a target thickness profile for each region.

2. A method of controlling surface non-uniformity of a wafer in a polishing operation, comprising:

a) providing a model for a wafer polishing that defines a plurality of regions on a wafer and identifies a wafer material removal rate in a polishing step of a polishing process for each of the regions, wherein the polishing process comprises a plurality of polishing steps;

b) polishing a wafer using a first polishing recipe based upon an incoming wafer thickness profile;

c) determining a wafer thickness profile for the post-polished wafer of step (b); and

d) calculating an updated polishing recipe based upon the wafer thickness profile of step (c) and the model of step (a) to maintain a target wafer thickness profile.

3. The method of claim 2, wherein the first polishing recipe is based on the model of step (a) to obtain the target wafer thickness profile.

4. The method of claim 2, wherein the first polishing recipe is determined empirically.

5. The method of claim 1 or 2, wherein the plurality of regions in the model of step (a) comprises regions extending radially outward from a center point on the wafer.

6. The method of claim 5, wherein the model comprises four or more regions.

7. The method of claim 1, wherein the polishing of step (b) comprises polishing the wafer at a plurality of polishing stations.

8. The method of claim 7, wherein the polishing step is carried out at three polishing stations.

9. The method of claim 7, wherein the polishing recipe at at least two polishing stations is the same.

10. The method of claim 7, wherein the polishing recipe at at least two polishing stations is different.

11. The method of claim 7, wherein the calculating the updated polishing recipe of step (c) comprises calculating updated polishing recipes for each of the plurality of polishing stations.

12. The method of claim 11, wherein the updated polishing recipes for each of the plurality of polishing stations accounts for the tool state of the individual polishing stations.

13. The method of claim 9 or 10, wherein the polishing of step (b) is carried out at a plurality of polishing stations, and wherein the wafer thickness profile for each of the subsequent polishing stations provided by the prediction from previous stations.

14. The method of claim 1 or 2, wherein the step of providing a model comprises:

(e) measuring pre-polished wafer thickness in each of a plurality of regions defined on one or more wafers;

(f) polishing the one or more wafers, wherein polishing comprises polishing the one or more wafers in a plurality of polishing steps;

(g) measuring the wafer material removal rate for the one or more wafers at each of the plurality of regions after each of the polishing steps of step (g);

(h) providing a model defining the effect of tool state on polishing effectiveness; and

(i) recording the pre-polished and post-polished wafer thicknesses for each or the regions on a recordable medium.

15. The method of claim 14, further comprising:

fitting the data to a linear or non-linear curve that establishes a relationship between the material removal rate of a region of the wafer and a polishing parameter of interest.

16. The method of claim 14, wherein the polishing parameter comprises polishing time.

17. The method of claim 16, wherein the polishing parameters further comprise a parameter selected from the group consisting of polishing time, polishing pad down forces and velocity, slurry flow and composition, conditioning time, conditioning disk down forces and velocity, oscillating speeds of both the conditioning disk and the wafer carrier.

18. The method of claim 1 or 2, wherein the wafer removal for a region $j$ ($AR'_j$) in the model of step (a) is determined according to the equation:

$$AR'_j = (c_{11j} \cdot x_1 + c_{12j}) \cdot t_1 + (c_{21j} \cdot x_2 + c_{22j}) \cdot t_2 + (c_{31j} \cdot x_3 + c_{32j}) \cdot t_3 + (c_{41j} \cdot x_1 + c_{42j}) \cdot t_4 + (c_{51j} \cdot x_5 + c_{52j}) \cdot t_5,$$

where $x_1$, $x_2$, $x_3$, $x_4$, and $x_5$ are the additional parameter values for polishing steps 1, 2, 3, 4, and 5, respectively; $t_1$, $t_2$, $t_3$, $t_4$, and $t_5$ are the polishing times for polishing steps 1, 2, 3, 4, and 5, respectively, and $c_{a1j}$ provides the contribution to wafer removal of the variable $x$ in polishing step $a$ in region $j$; and $c_{a2j}$ provides the contribution to wafer removal of polishing time in polishing step $a$.

19. The method of claim 18 wherein the wafer material removal rate profile accounts for tool state by scaling the profile using the scaling factor:

$$\left(1 + k_p \cdot t_p + k_d \cdot t_d + k_{pd} \cdot t_p \cdot t_d\right),$$

where the terms $t_p$ and $t_d$ refer to pad and disk life, respectively, with units of hour; and the terms $k_p$, $k_d$ and $k_{pd}$ are empirically determined coefficients relating pad and disk life to removal rate.

20. The method of claim 2, wherein updated polishing recipe is attained by solving the equation:

$$\min_x f\left(y^{sp}, g(x)\right)$$

where $x$ is a vector of times and other processing parameters corresponding to the polishing recipe; $g(x)$ is the model for the polishing process, $y^{sp}$ is a vector of the desired average region wafer thicknesses; and $f(y^{sp}, g(x))$ is a penalty function to penalize the deviation between the model predictions $g(x)$ and the desired thicknesses $y^{sp}$.

21. A method of determining a model for wafer thickness profile, comprising:

(a) measuring pre-polished wafer thickness in each of a plurality of regions defined on one or more wafers;

(b) polishing the one or more wafers, wherein polishing comprises polishing the one or more wafers in a plurality of polishing steps;

(c) measuring the wafer material removal rate for the one or more wafers at each of the plurality of regions after each of the polishing steps of step (b);

(d) providing a model defining the effect of tool state on polishing effectiveness; and

(e) recording the pre-polished and post-polished wafer thicknesses for each or the regions on a recordable medium.

22. The method of claim 21, further comprising:

fitting the data to a linear or non-linear curve that establishes a relationship between the material removal rate of a region of the wafer and a polishing parameter of interest.

23. The method of claim 22, wherein the polishing parameter comprises polishing time.

24. The method of claim 23, wherein the polishing parameters further comprise a parameter selected from the group consisting of polishing time, polishing pad down forces and velocity, slurry flow and composition, conditioning time, conditioning disk down forces and velocity, oscillating speeds of both the conditioning disk and the wafer carrier.

25. The method of claim 21 wherein the wafer material removal for a region *j* ($AR'_j$) in the model of step (a) is determined according to the equation:

$$AR'_j = (c_{11j} \cdot x_1 + c_{12j}) \cdot t_1 + (c_{21j} \cdot x_2 + c_{22j}) \cdot t_2 + (c_{31j} \cdot x_3 + c_{32j}) \cdot t_3 + (c_{41j} \cdot x_1 + c_{42j}) \cdot t_4 + (c_{51j} \cdot x_5 + c_{52j}) \cdot t_5,$$

where $x_1$, $x_2$, $x_3$, $x_4$, and $x_5$ are the additional parameter values for polishing steps 1, 2, 3, 4, and 5, respectively; $t_1$, $t_2$, $t_3$, $t_4$, and $t_5$ are the polishing times for polishing steps 1, 2, 3, 4, and 5, respectively, and $c_{a1j}$ provides the contribution to wafer removal of the variable $x$ in polishing step $a$ in region $j$; and $c_{a2j}$ provides the contribution to wafer removal of polishing time in polishing step $a$.

26. The method of claim 21 wherein the wafer material removal rate profile accounts for tool state by scaling the profile using the scaling factor:

$$\left(1+k_p \cdot t_p + k_d \cdot t_d + k_{pd} \cdot t_p \cdot t_d\right),$$

where the terms $t_p$ and $t_d$ refer to pad and disk life, respectively, with units of hour; and the terms $k_p$, $k_d$ and $k_{pd}$ are empirically determined coefficients relating pad and disk life to removal rate.

27. The method of claim 22, wherein a the model is determined using less than 10 wafers.

28. An apparatus for conditioning polishing pads used to planarize substrates, comprising:

a carrier assembly having a plurality of arms for holding a wafer positionable over a plurality of planarizing surfaces of a plurality of polishing pads;

controlling means capable of controlling an operating parameter of the polishing process; and

a controller operatively coupled to the controlling means, the controller operating the controlling means to adjust the operating parameter of the polishing process as a function of a model for a wafer thickness profile, the model comprising:

defining a polishing model that defines a plurality of regions on a wafer and identifies a wafer material removal rate in a polishing step of a polishing process for each of the regions, wherein the polishing process comprises a plurality of polishing steps.

29. The apparatus of claim 28, wherein the model defines wafer removal for a region $j$ ($AR'_j$) in the wafer material removal rate model is determined according to the equation:

$$AR'_j = (c_{11j} \cdot x_1 + c_{12j}) \cdot t_1 + (c_{21j} \cdot x_2 + c_{22j}) \cdot t_2 + (c_{31j} \cdot x_3 + c_{32j}) \cdot t_3 + (c_{41j} \cdot x_1 + c_{42j}) \cdot t_4 + (c_{51j} \cdot x_5 + c_{52j}) \cdot t_5,$$

where $x_1$, $x_2$, $x_3$, $x_4$, and $x_5$ are the additional parameter values for polishing steps 1, 2, 3, 4, and 5, respectively; $t_1$, $t_2$, $t_3$, $t_4$, and $t_5$ are the polishing times for polishing steps 1, 2, 3, 4, and 5, respectively, and $c_{a1j}$ provides the contribution to wafer removal of the variable $x$ in polishing step $a$ in region $j$; and $c_{a2j}$ provides the contribution to wafer removal of polishing time in polishing step $a$.

30. A computer readable medium comprising instructions being executed by a computer, the instructions including a computer-implemented software application for a chemical mechanical polishing process, the instructions for implementing the process comprising:

a) receiving data from a chemical mechanical polishing tool relating to the wafer removal rate of at least one wafer processed in the chemical mechanical polishing process; and

b) calculating, from the data of step (a), updated polishing recipe, wherein the updated polishing recipe is calculated by determining the difference between an output of a wafer material removal rate model and the data of step (a).

31. The medium of claim 28, wherein the model for a wafer material removal rate defines a plurality of regions on a wafer and identifies a wafer material removal rate in a polishing step of a polishing process for each of the regions, wherein the polishing process comprises a plurality of polishing steps.

32. The medium of claim 30, wherein the wafer removal for a region $j$ ($AR'_j$) in the wafer material removal rate model is determined according to the equation:

$$AR'_j = (c_{11j} \cdot x_1 + c_{12j}) \cdot t_1 + (c_{21j} \cdot x_2 + c_{22j}) \cdot t_2 + (c_{31j} \cdot x_3 + c_{32j}) \cdot t_3 + (c_{41j} \cdot x_1 + c_{42j}) \cdot t_4 + (c_{51j} \cdot x_5 + c_{52j}) \cdot t_5,$$

where $x_1$, $x_2$, $x_3$, $x_4$, and $x_5$ are the additional parameter values for polishing steps 1, 2, 3, 4, and 5, respectively; $t_1$, $t_2$, $t_3$, $t_4$, and $t_5$ are the polishing times for polishing steps 1, 2, 3, 4, and 5, respectively, and $c_{a1j}$ provides the contribution to wafer removal of the variable $x$ in

polishing step $a$ in region $j$; and $c_{a2j}$ provides the contribution to wafer removal of polishing time in polishing step $a$.